Notice of Allowability	Application No.	Applicant(s)	
	10/625,027	KIM ET AL.	
	Examiner	Art Unit	
	Pamela E Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the filing of the election on 13 September 2004*.

2. ☒ The allowed claim(s) is/are *8-21*.

3. ☒ The drawings filed on *22 July 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

DETAILED ACTION

This office action is in response to the filing of the election on 13 September 2004. Claims 1-21 are pending; claims 1-7, 18 and 19 have been withdrawn from consideration.

Election/Restrictions

Applicant's election with traverse of group II, claims 8-17, 20 and 21 in the reply filed on 13 September 2004 is acknowledged. The traversal is on the ground(s) that the restriction requirement lacks reason and/or examples supporting a showing of the burden upon the office to examine both inventions at the same time. Therefore, in light of M.P.E.P. § 803, the requirement should be remove.

This is not found persuasive because the "assumption" that a close relationship exists between the two inventions is apparent, however this in itself does not overcome the restriction requirement. According to M.P.E.P. § 803, the proper criteria between for a restriction is (1) the inventions must be independent and separate and (2) there must be serious burden on the Examiner if the restriction is not required. The product and the process of manufacturing a semiconductor device are considered to be separate and independent by the Office. They are classified in two different art classifications and assigned two different sets of Art Units. It would be a serious burden on the Examiner to examine two such distinct inventions despite the fact that they are so closely related.

Claims 1-7, 18 and 19 are withdrawn from further consideration by the Examiner, 37 C.F.R. § 1.142(b), as being drawn to a non-elected invention, the requirement having been traversed in the reply filed on 13 September 2004.

The requirement is still deemed proper and is therefore made FINAL.

Allowable Subject Matter

Claims 8-21 are allowed.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance: prior art does not anticipate, teach, or suggest a method of fabricating a semiconductor device where conductive patterns are formed by depositing a conductive layer and a capping layer on an insulating layer disposed on a semiconductor substrate; filling at least one space between at least two adjacent conductive patterns by depositing a first interlayer insulating layer in the at least one space; exposing a part of a sidewall of the capping layer by wet etching the first interlayer insulating layer without damaging the capping layer; forming a first spacer on an exposed part of the sidewall of the capping layer; forming a second interlayer insulating layer on the first interlayer insulating layer, the capping layer and the first spacer, and planarizing a top surface of the second interlayer insulating layer; forming a contact hole between the at least two adjacent conductive patterns, wherein the contact hole is self-aligned with the capping layer, by dry etching the second interlayer insulating layer, the first interlayer insulating layer, and the

insulating layer; forming a second spacer in an innerwall of the contact hole; and forming a contact plug electrically connected to the semiconductor substrate by filling the contact hole with conductive material.

For example, Uh et al. (6,391,736) disclose a method of fabricating a semiconductor device where conductive patterns are formed by depositing a conductive layer (206) and a capping layer (208) on an insulating layer (204) disposed on a semiconductor substrate (100); filling at least one space between at least two adjacent conductive patterns by depositing a first interlayer layer (304) in the at least one space; exposing a part of a sidewall of the capping layer (208) by wet etching; forming a first spacer (302) on an exposed part of the sidewall of the capping layer (208) (Fig. 4; col. 8, lines 1-44); forming a second interlayer insulating layer (306) on the first interlayer layer (304), the capping layer (208) and the first spacer (302), and planarizing a top surface of the second interlayer insulating layer (306); forming a contact hole (307) between the at least two adjacent conductive patterns, wherein the contact hole (307) is self-aligned with the capping layer (208), by etching the second interlayer insulating layer (308) and the insulating layer (204) (Fig. 5; col. 8, line 60 thru col. 9, line 6); forming a second spacer (308) in an innerwall of the contact hole (307) (Fig. 6; col. 9, lines 7-15); and forming a contact plug electrically connected to the semiconductor substrate (100) by filling the contact hole (307) with conductive material (400) (Fig. 7; col. 9, lines 16-30).

However, Uh et al. do not disclose, anticipate, teach, or suggest exposing a part of a sidewall of the capping layer by wet etching the first interlayer insulating layer without damaging the capping layer.

Park (6,709,672) discloses a method of fabricating a semiconductor device where conductive patterns are formed by depositing a conductive layer (174) and a capping layer (176) on an insulating layer (140) disposed on a semiconductor substrate (105) (Fig. 6A; col. 7, lines 33-55); filling at least one space between at least two adjacent conductive patterns (174) by depositing a first interlayer insulating layer (150) in the at least one space (Fig. 6B; col. 7, lines 56-64); forming a first spacer (172) on an exposed part of the sidewall of the capping layer (176); forming a contact hole (190) between the at least two adjacent conductive patterns (174), wherein the contact hole (190) is self-aligned with the capping layer (176), by dry etching the first interlayer insulating layer (150), and the insulating layer (140) (Fig. 7A & 7B; col. 8, lines 8-30); forming a second spacer (194) in an innerwall of the contact hole (190) (col. 9, lines 13-19); and forming a contact plug (195) electrically connected to the semiconductor substrate (105) by filling the contact hole (190) with conductive material (col. 10A & 10B; col. 9, lines 1-36).

However, Park does not disclose, anticipate, teach or suggest exposing a part of a sidewall of the capping layer by wet etching the first interlayer insulating layer without damaging the capping layer and forming a second interlayer insulating layer on the first interlayer insulating layer, the capping layer and the first spacer, and planarizing a top surface of the second interlayer insulating layer.

The prior art made of record in this action does not anticipate, teach, or suggest a method of fabricating a semiconductor device where conductive patterns are formed by depositing a conductive layer and a capping layer on an insulating layer disposed on a semiconductor substrate; filling at least one space between at least two adjacent conductive patterns by depositing a first interlayer insulating layer in the at least one space; exposing a part of a sidewall of the capping layer by wet etching the first interlayer insulating layer without damaging the capping layer; forming a first spacer on an exposed part of the sidewall of the capping layer; forming a second interlayer insulating layer on the first interlayer insulating layer, the capping layer and the first spacer, and planarizing a top surface of the second interlayer insulating layer; forming a contact hole between the at least two adjacent conductive patterns, wherein the contact hole is self-aligned with the capping layer, by dry etching the second interlayer insulating layer, the first interlayer insulating layer, and the insulating layer; forming a second spacer in an innerwall of the contact hole; and forming a contact plug electrically connected to the semiconductor substrate by filling the contact hole with conductive material.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP

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